AMENDMENTS TO THE SPECIFICATION

Please amend the paragraphs beginning on page 1, lines 10-19 as follows:

In recent years, semiconductor devices have become more integrated, and structures of semiconductor elements have become more complicated. Further, the number of layers in multilayer interconnects used for a logical system has ~~been~~ increased. Accordingly, irregularities on a surface of a semiconductor device are increased, so that step heights on the surface of the semiconductor device tend to be large. This is because, in a manufacturing process of a semiconductor device, a thin film is formed on a semiconductor device, then micromachining processes, such as patterning or forming holes, are performed on the semiconductor device, and these processes are repeated to form subsequent thin films on the semiconductor device.

When the number of irregularities is increased on a surface of a semiconductor device, the following problems arise. When a thin film is formed on a semiconductor device, the thickness of the film formed at portions having a step is relatively small. Further, an open circuit may be caused by disconnection of interconnects, or a short circuit may be caused by insufficient insulation between interconnect layers. As a result, good products cannot be obtained, and the yield tends to be lowered. Further, even if a semiconductor device initially works normally, reliability of the semiconductor device is lowered after ~~a long-term~~long-term use. At the time of exposure in a lithography process, if the irradiation surface has irregularities, then a lens unit in an exposure system is locally unfocused. Therefore, if the irregularities of the surface of the semiconductor device are increased, then it becomes problematically difficult to form a fine pattern itself on the semiconductor device.

Please amend the paragraph beginning on page 3, line 18 as follows:

A polishing pad having a two-layer structure in which a relatively hard polyurethane foam layer is attached to a relatively soft non-woven fabric is effective in reducing an influence

due to nanotopology, i.e., swell of a surface of a substrate. ~~There has been well known a polishing pad~~A polishing pad having a two-layer layer ~~structure~~ structure, such as IC-1000/SUBA400 manufactured by Rodel ~~Inc.~~Inc., is well known. In order to remove polishing wastes attached to a surface of the polishing pad during CMP, pad conditioning is conducted to remove a portion of the surface of the polishing pad with a diamond disk. As a result of the pad conditioning, a depth of the grooves formed in the surface of the polishing pad and a ratio of a soft layer and a hard layer change with time according to abrasion of the polishing pad, thereby exerting a great influence on the polishing process.

Please amend the paragraphs beginning on page 4, lines 10-16 as follows:

The present invention has been made in view of the above drawbacks. ~~It is, therefore,~~It is an object of the present invention to provide a polishing apparatus and a substrate polishing method which can polish a substrate with accuracy so as to have a desired film thickness, can prevent a manufacturing yield from being lowered by excessively polishing, and can prevent manufacturing cost from being increased by reworking processes.

A second object of the present invention is to provide a polishing method and a polishing apparatus which can properly control a polishing rate and polishing properties which would change due to a depth of a groove formed in a surface of a polishing pad, a thickness of a hard polishing pad, a state of a surface of a dressed polishing pad, or a temperature of a surface of a polishing pad, which can prevent reworking due to excessive polishing, and which can reduce a risk of a lowered yield.

Please amend the sub-heading on page 10, line 5 as follows:

~~Best Mode for Carrying Out the Invention~~Detailed Description of the Invention

Please amend the paragraph beginning on page 27, line 11 as follows:

The present invention is suitable for use in a polishing apparatus and includes a polishing method for polishing a substrate such as a semiconductor wafer to a flat mirror finish.